7. (amended) A method for manufacturing a semiconductor device having a trench isolation region according to claim 1, wherein the trench includes sidewall surfaces and a bottom surface, the method further comprising of thermally oxidizing the sidewall surfaces and the bottom surface of the trench to form a thermal oxide layer thereon, wherein the dielectric layer is formed in direct contact with the thermal oxide layer.

B2

14. (amended) A method for manufacturing a semiconductor device having a trench isolation region, the method comprising:

forming a trench in a semiconductor layer;

forming a dielectric layer in the trench;

heating the dielectric layer at a temperature of at least 1050°C; and

forming a well in the semiconductor layer adjacent to the trench after the heating the dielectric layer at a temperature of at least 1050°C.

B3

C1

19. (amended) A method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

forming a first layer on a semiconductor substrate;

forming a polishing stopper layer above the first layer;

forming at least one trench by etching the first layer while using the polishing stopper layer as a mask;

forming a dielectric layer in and above the trench;

planarizing the dielectric layer using the polishing stopper layer as a stopper;

heating the dielectric layer to a temperature of at least 1050°C; and

after the heating the dielectric layer to a temperature of at least 1050°C, forming a well in the semiconductor substrate adjacent to the trench.

B4

Please add new claims 32-37 as follows:

--32. A method for manufacturing a semiconductor device, comprising:

providing a semiconductor layer;

forming a plurality of trenches in the semiconductor layer;

forming a thermal oxide layer on the semiconductor surface in the trenches;

depositing a dielectric layer into the trenches and filling the trenches with the dielectric layer;

thermally treating the dielectric layer in the trenches at a temperature of at least 1050°C; and

after the thermally treating the dielectric layer in the trenches, forming a well region between adjacent trenches.

33. A method according to claim 32, wherein the dielectric layer is formed in direct contact with the thermal oxide layer in the trenches.

34. A method according to claim 33, wherein the dielectric layer is formed with a film density of at least 2.1g/cm^3.

35. A method according to claim 34, wherein the dielectric layer is formed by a high density plasma CVD method.

36. A method according to claim 35, wherein the semiconductor layer comprises an epitaxial growth layer formed on a semiconductor substrate.

37. A method according to claim 36, wherein the epitaxial growth layer has a thickness of at least 2 μm.--